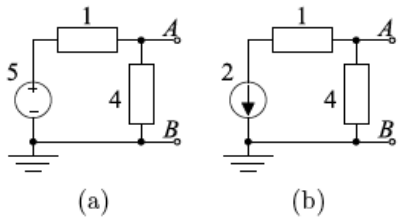
Design Engineering – EA1.3 Electronics

Problem Sheet 3 (Topics 7 - 8)

Key: [A] = easy …… [E] = hard

1. [B] Calculate the Thévenin equivalent networks at the terminals A and B for each of the following.



2. [B] Use nodal analysis to calculate an expression for A in Fig. 2 in terms of I and then rearrange this to give I in terms of A. Show how these expressions are related to the Thévenin equivalent networks at the terminals A and B.

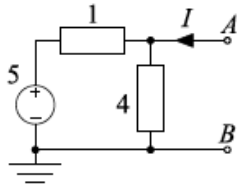


Figure 2

3. [C] Calculate the Thévenin equivalent networks at the terminals A and B in Fig. 3 in two ways: (a) by combining resistors to simplify the circuit, and (b) by using nodal analysis to express A in terms of I.

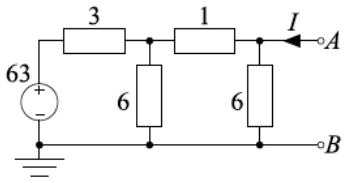


Figure 3

4. [C] Find the current I in Fig. 4 in two ways: (a) by nodal analysis and (b) by combining the leftmost three components into their Thevenin equivalent.

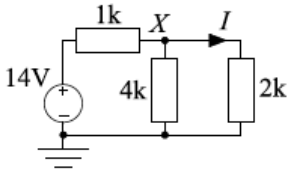


Figure 4

5. [C] For what value of R in Fig. 5 will the power dissipation in R be maximized. Find the power dissipation in R in this case.

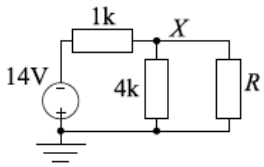


Figure 5

6. [C] Find the Thévenin equivalent of the circuit shown in Fig. 6 between nodes A and B by using superposition to find the open-circuit voltage and combining resistors to find the Thevenin resistance.

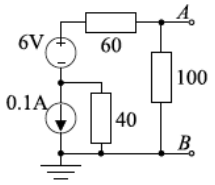


Figure 6

7. [B] Draw a dimensioned sketch of the waveform of i in the circuit of Fig. 7(a) when v has the waveform shown in Fig. 7(b).

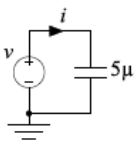


Figure 7 (a)

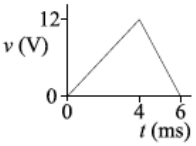


Figure 7 (b)

8. [D] In the circuit of Fig. 11, the output logic levels from the inverter are 0V and 5V and the inverter has a maximum output current of 2mA. The inverter senses a low voltage when its input is < 1.5 V. If x changes from logic 0 to logic 1, determine the delay until z changes. Ignore the inverter input currents and any delays inside the inverters themselves.

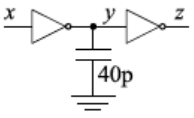


Figure 8